

Figure 1 is a schematic diagram of a multi-channel system architecture. The diagram shows a central horizontal bus labeled '1' with multiple channels (1-5) connected to it. Each channel contains a 'SYSTEM SLOT' (2) and a 'PERIPHERAL SLOT' (3). The system is connected to a 'J2' interface on the left and a 'J1' interface on the right. Various components are labeled with numbers 1 through 29, including slots, connectors, and internal components.

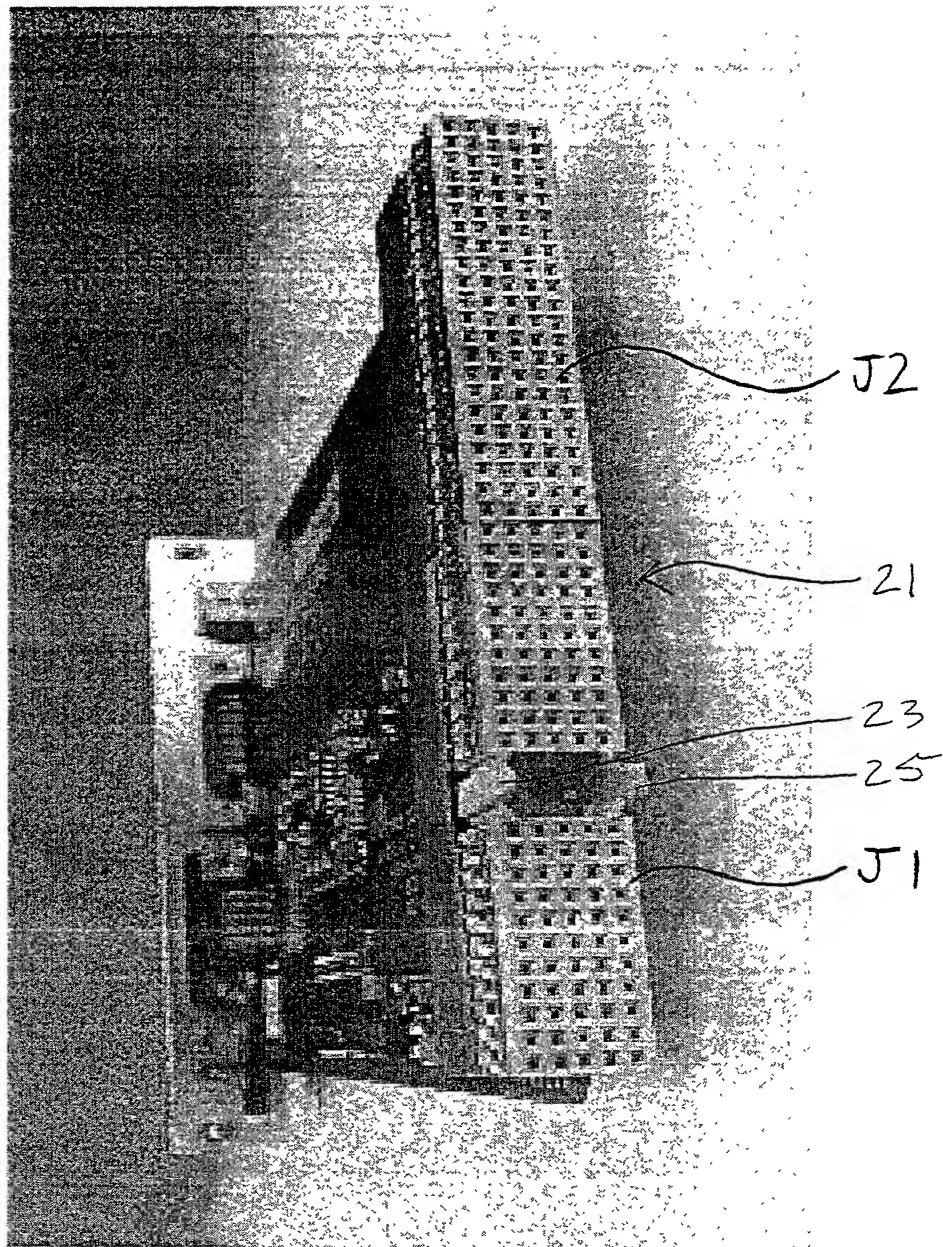


FIG. 2 (Prior Art)

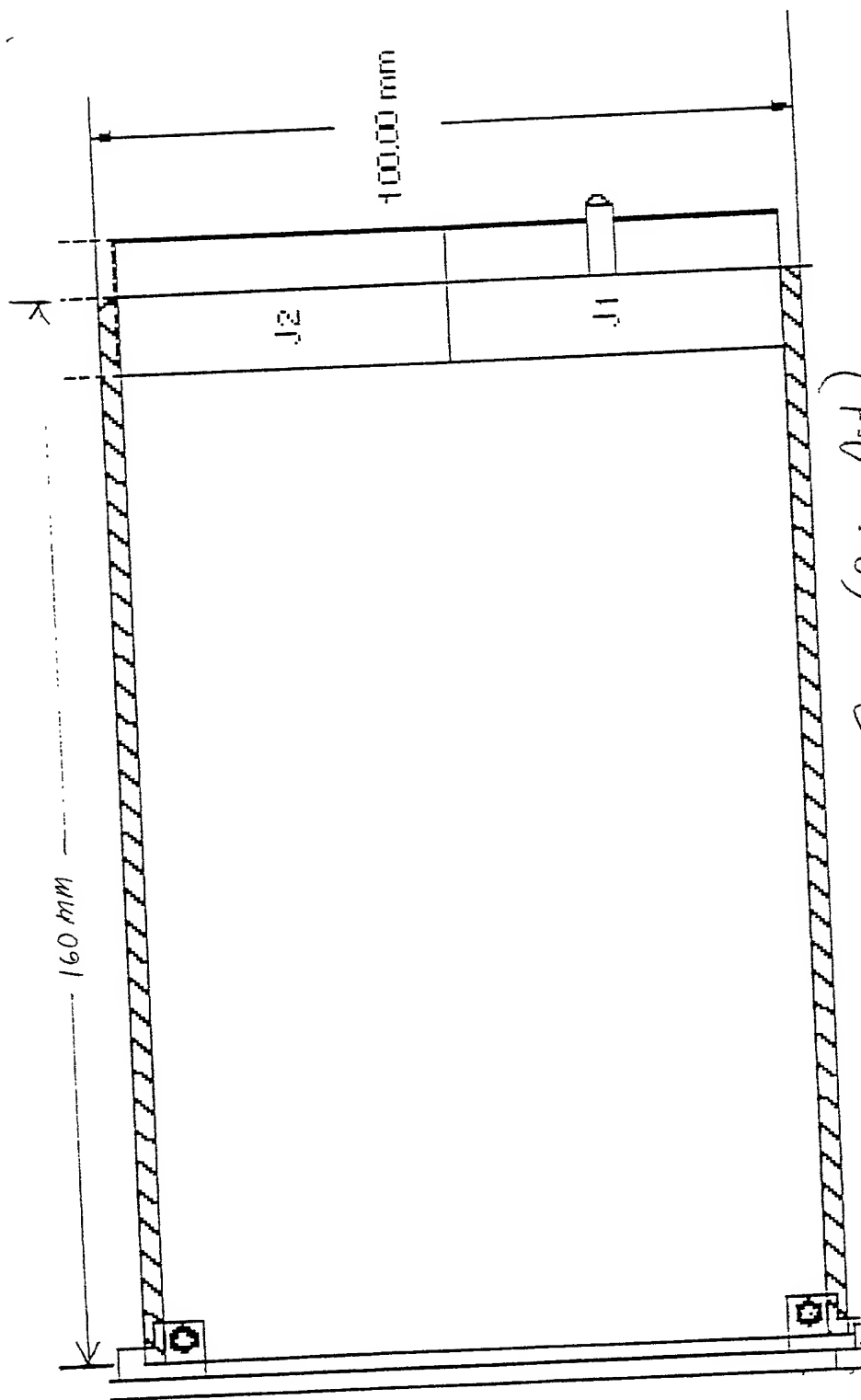
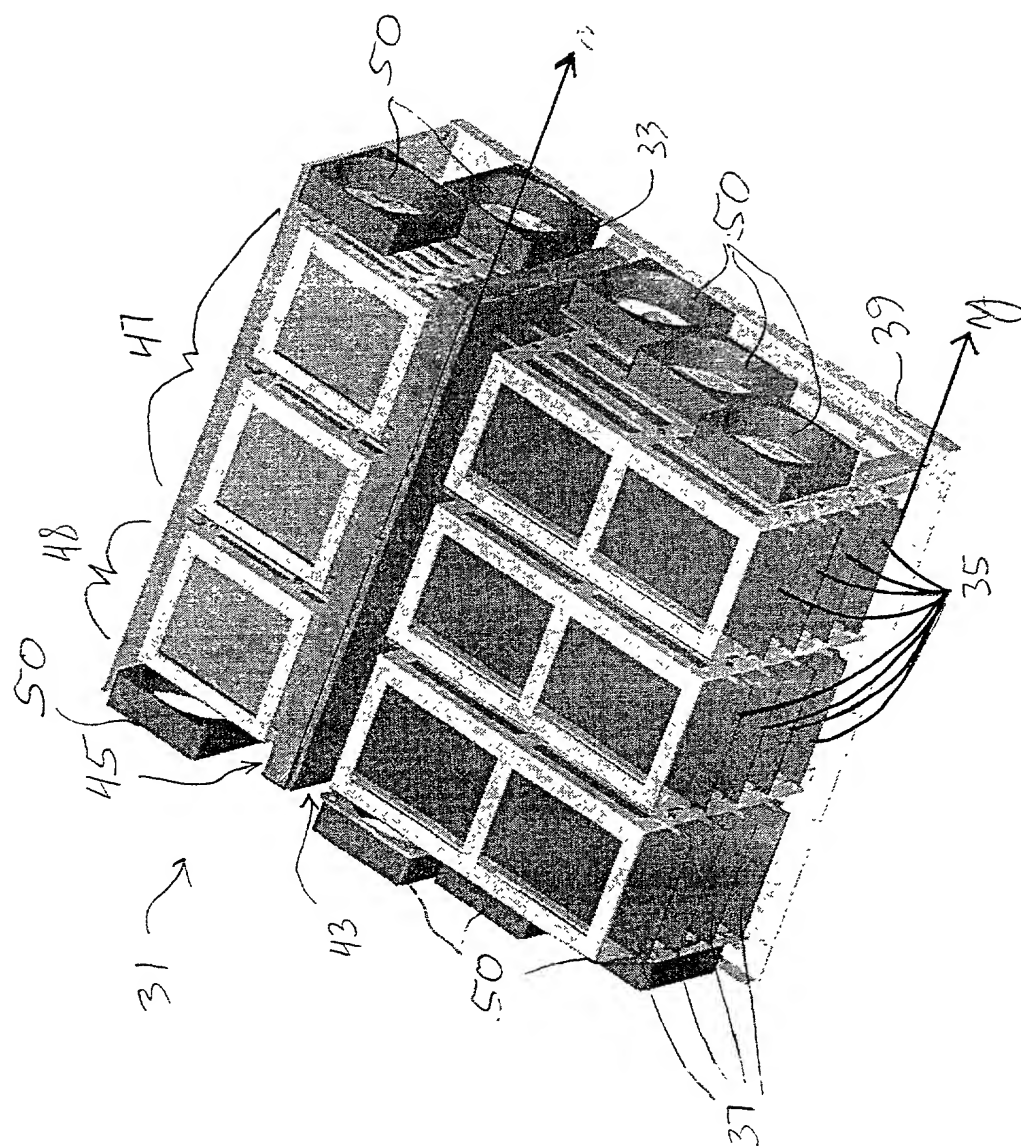


FIG. 3 (Prior Art)

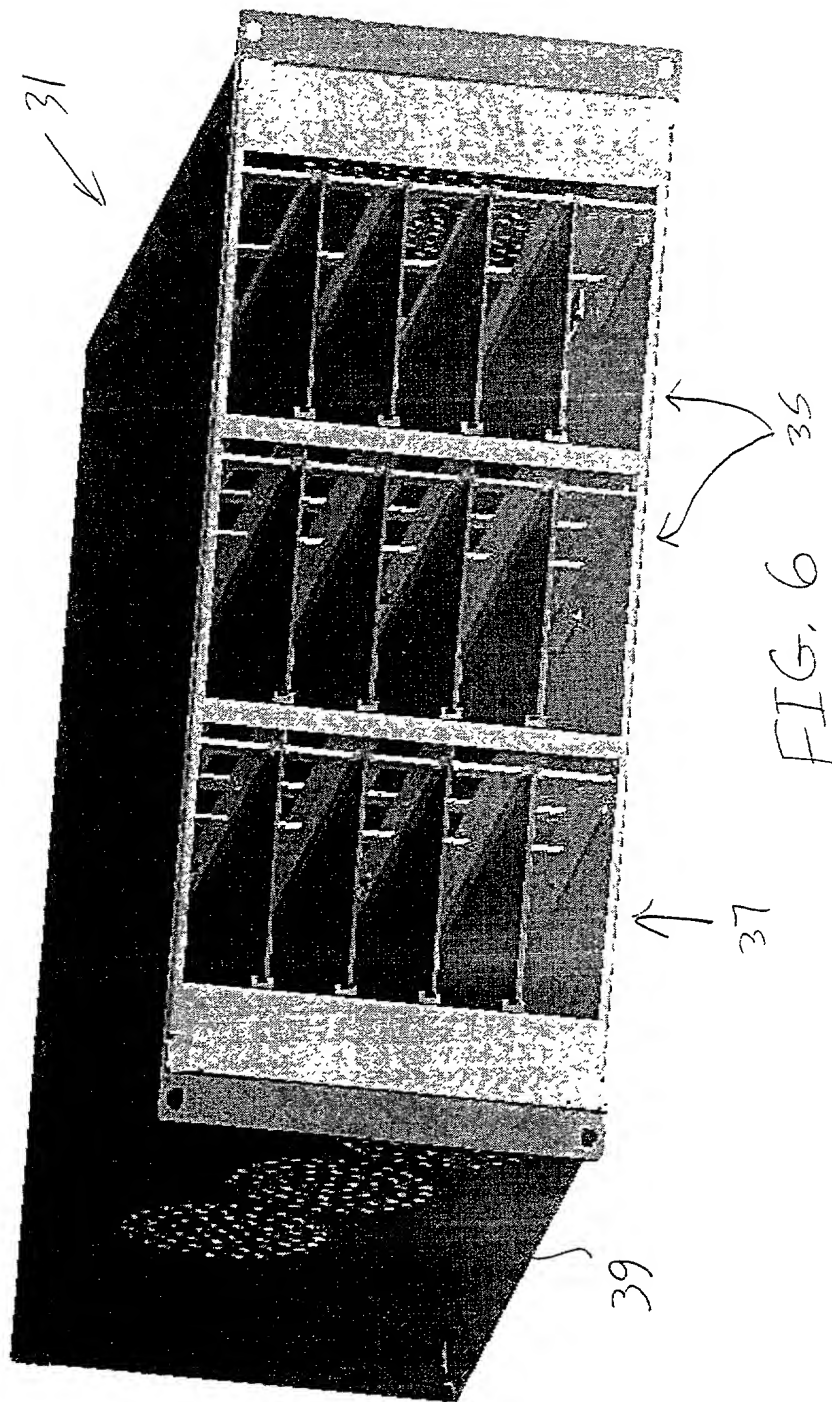
25	GND	5V	REQ64#	ENUM#	3.3V	5V	GND	J1	
24	GND	AD[1]	5V	V(I/O)	AD[0]	ACK64#	GND		
23	GND	3.3V	AD[4]	AD[3]	5V	AD[2]	GND		
22	GND	AD[7]	GND	3.3V	AD[6]	AD[5]	GND		
21	GND	3.3V	AD[9]	AD[8]	M66EN	C/BE[0]#	GND		
20	GND	AD[12]	GND	V(I/O)	AD[11]	AD[10]	GND		
19	GND	3.3V	AD[15]	AD[14]	GND	AD[13]	GND		
18	GND	SERR#	GND	3.3V	PAR	C/BE[1]#	GND		
17	GND	3.3V	SDONE	SBO#	GND	PERR#	GND		
16	GND	DEVSEL#	GND	V(I/O)	STOP#	LOCK#	GND		
15	GND	3.3V	FRAME#	IRDY#	GND	TRDY#	GND	CONNECTOR	
12-14	KEY AREA								
11	GND	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	GND		
10	GND	AD[21]	GND	3.3V	AD[20]	AD[19]	GND		
9	GND	C/BE[3]#	IDSEL	AD[23]	GND	AD[22]	GND		
8	GND	AD[26]	GND	V(I/O)	AD[25]	AD[24]	GND		
7	GND	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND		
6	GND	REQ#	GND	3.3V	CLK	AD[31]	GND		
5	GND	BRSVP1A5	BRSVP1B5	RST#	GND	GNT#	GND		
4	GND	BRSVP1A4	GND	V(I/O)	INTP	INTS	GND		
3	GND	INTA#	INTB#	INTC#	5V	INTD#	GND	RO	
2	GND	TCK	5V	TMS	TDO	TDI	GND		
1	GND	5V	-12V	TRST#	+12V	5V	GND		
Pin	Z	A	B	C	D	E	F		

FIG. 4



5165

FIG. 6 is a perspective view of the device 10 in a closed position.



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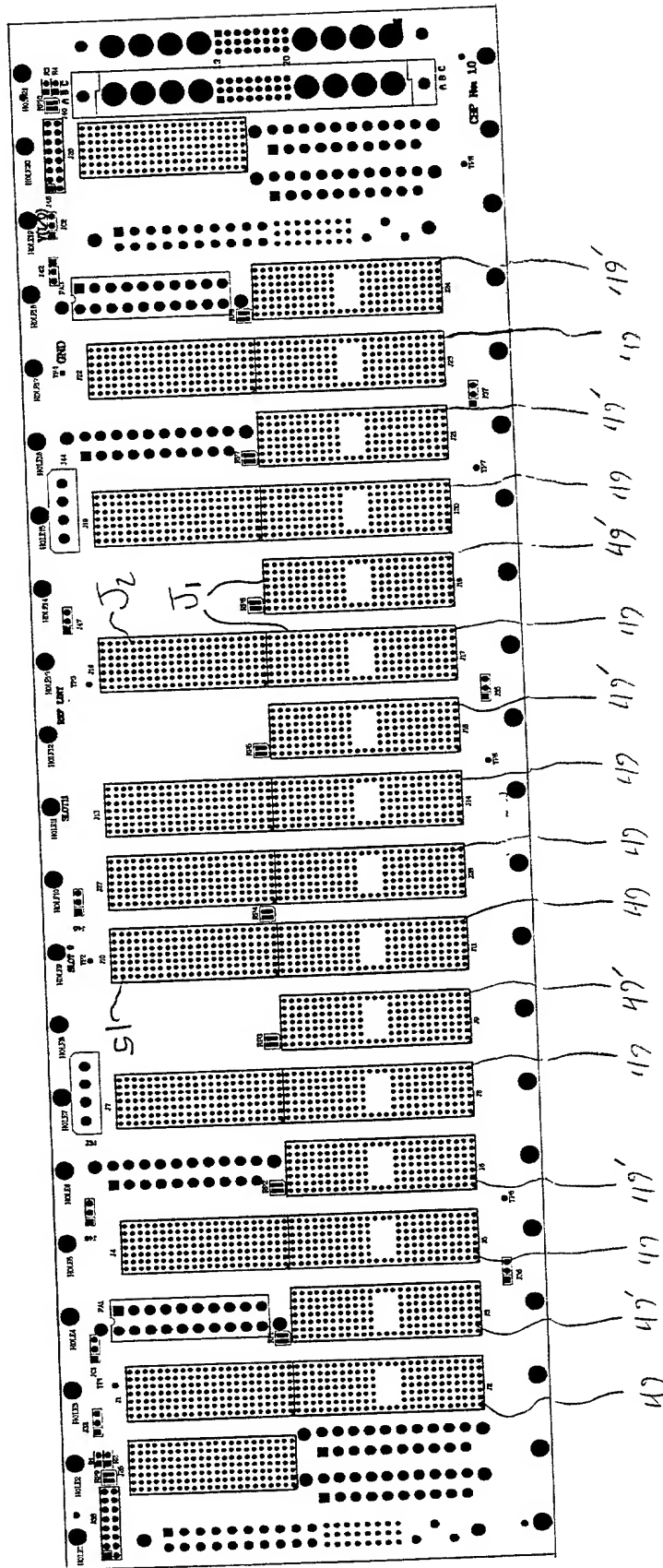


FIG. 7

FIG. 9 is a schematic diagram of a system architecture. The diagram shows a central horizontal bus labeled "12-100-Base T Bus, KVM Bus, Fiber Channel Bus and Power Supply". Above the bus, there are four main components: a "Up Link Fiber Channel Port" (69), a "USB Mouse" (85) and "USB Keyboard" (83) connected to a "Monitor" (83), and an "Up link 100 MB or GB Network Port" (63). Below the bus, there are four main components: a "73" (73), a "35" (35), a "61" (61), and a "35" (35). The "73" (73) is connected to the bus via a "55" (55) and "57" (57). The "35" (35) is connected to the bus via a "59" (59). The "61" (61) is connected to the bus via a "35" (35). The "35" (35) is connected to the bus via a "35" (35). Below these components, there are four "USB port" (79) components, each connected to a "77" (77) and "81" (81). The "77" (77) and "81" (81) are connected to the bus via a "53" (53). Below the "USB port" (79) components, there are four "75" (75) and "47" (47) components, each connected to the bus via a "75" (75) and "47" (47).

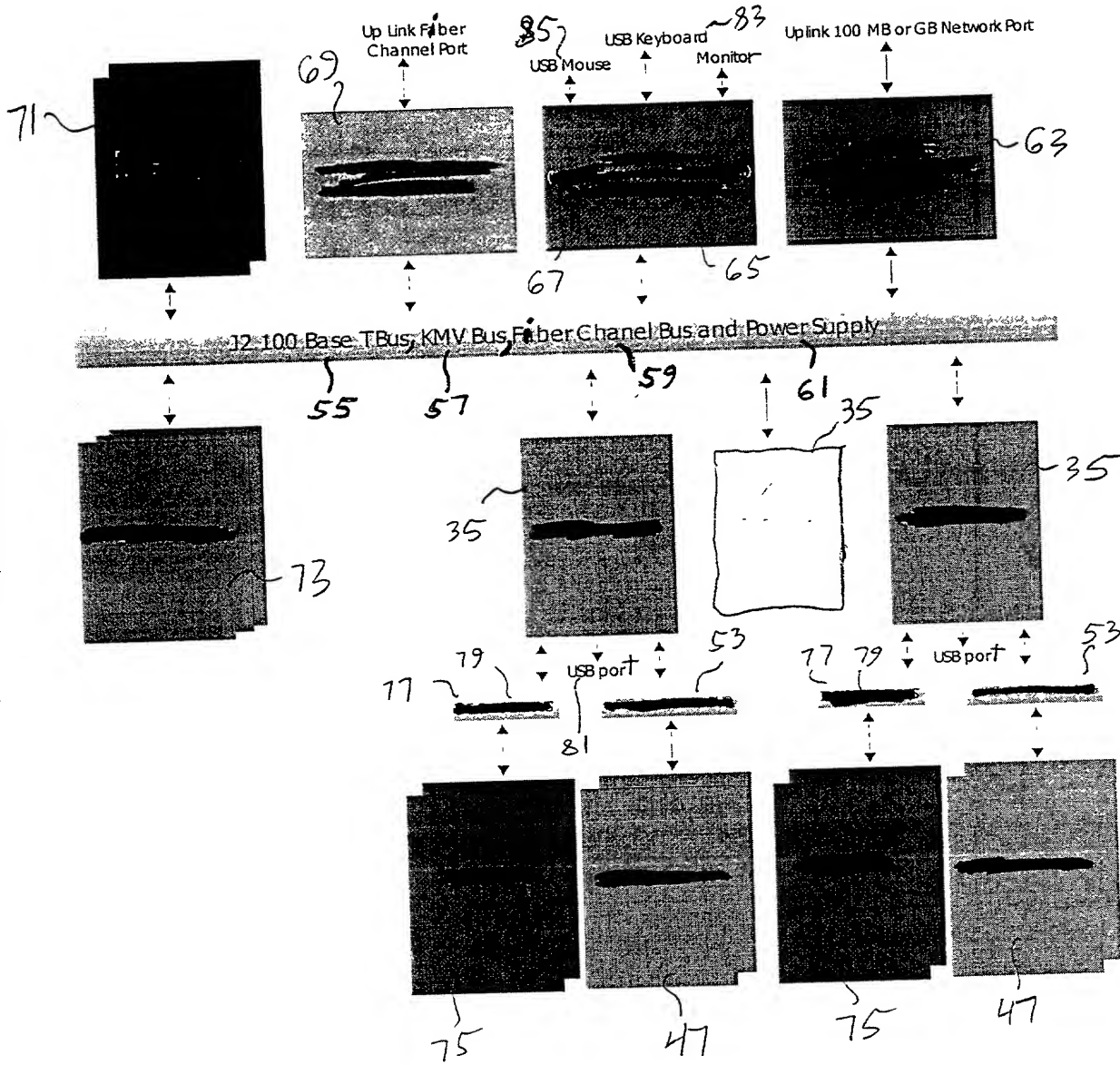


FIG. 9

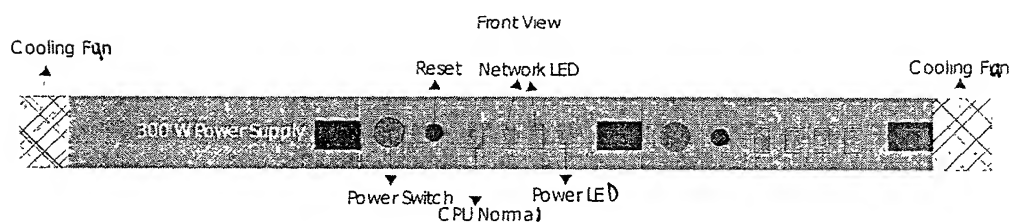
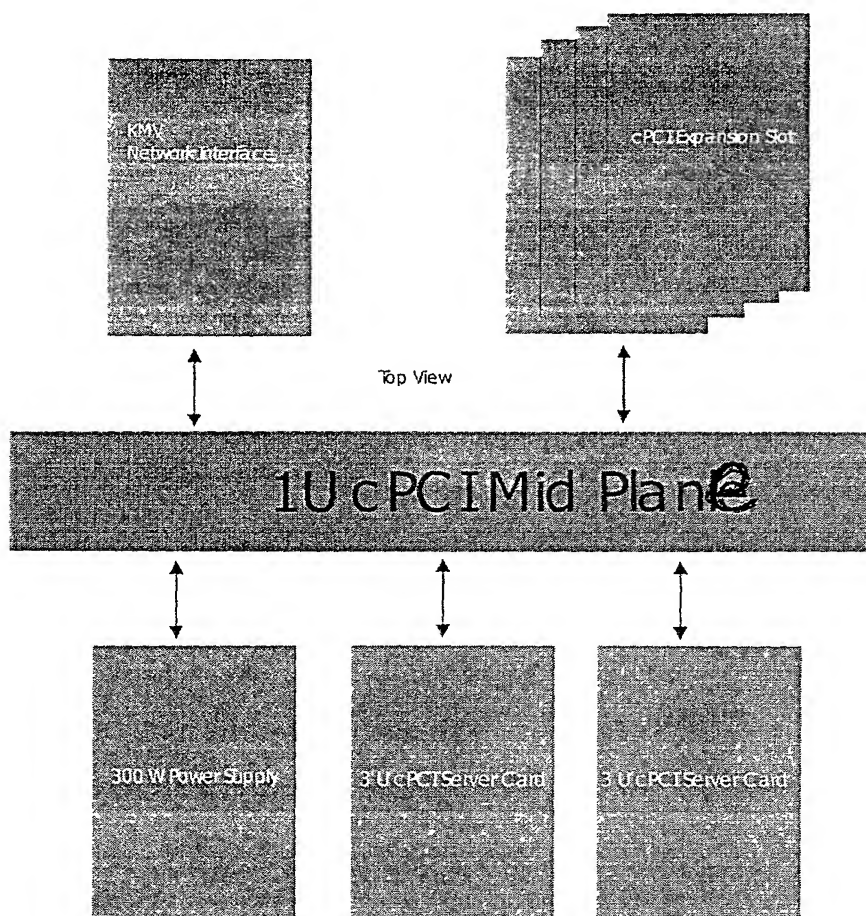
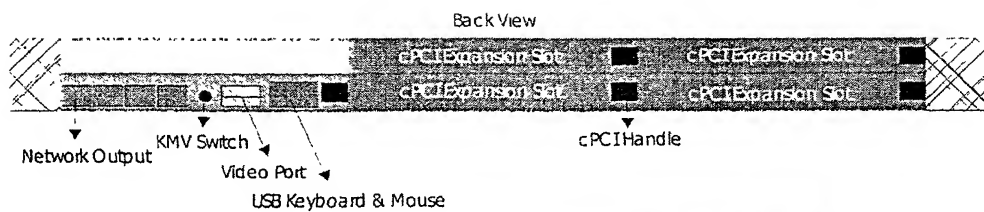


FIG. 11

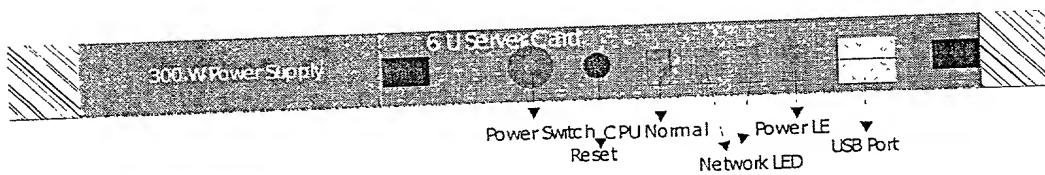
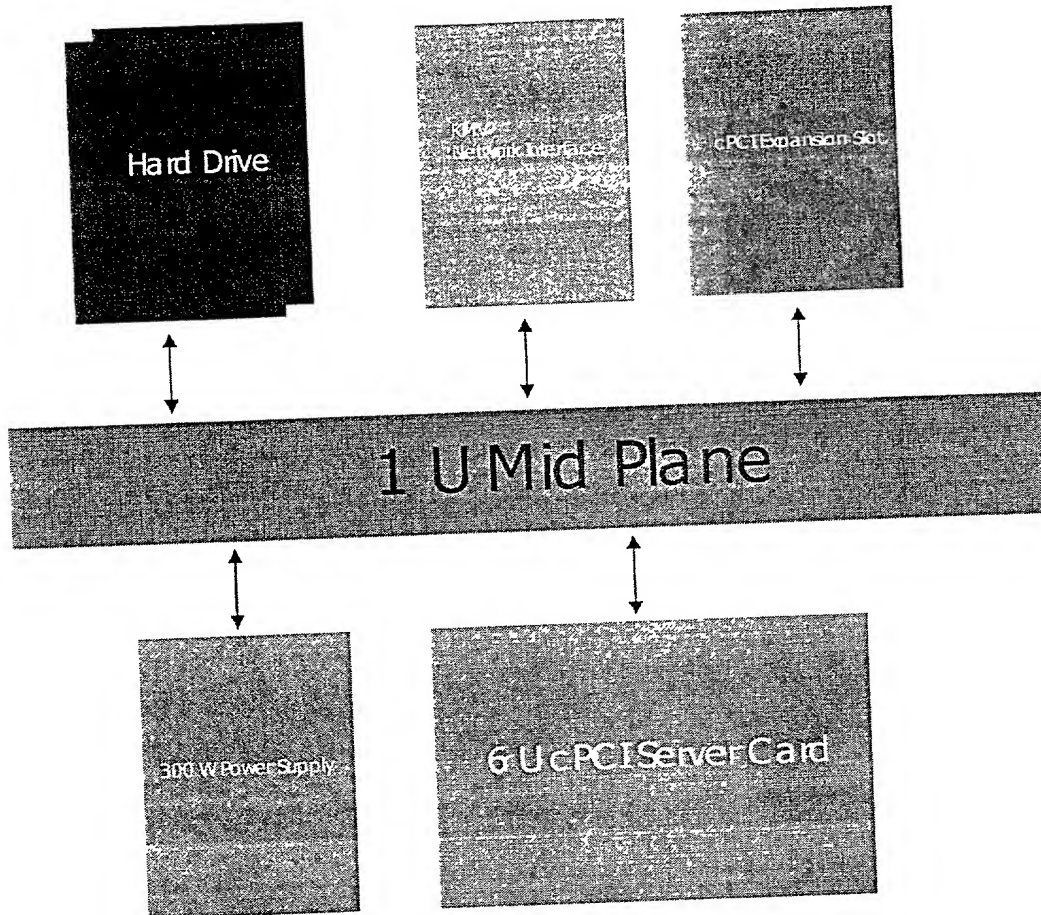


FIG. 12

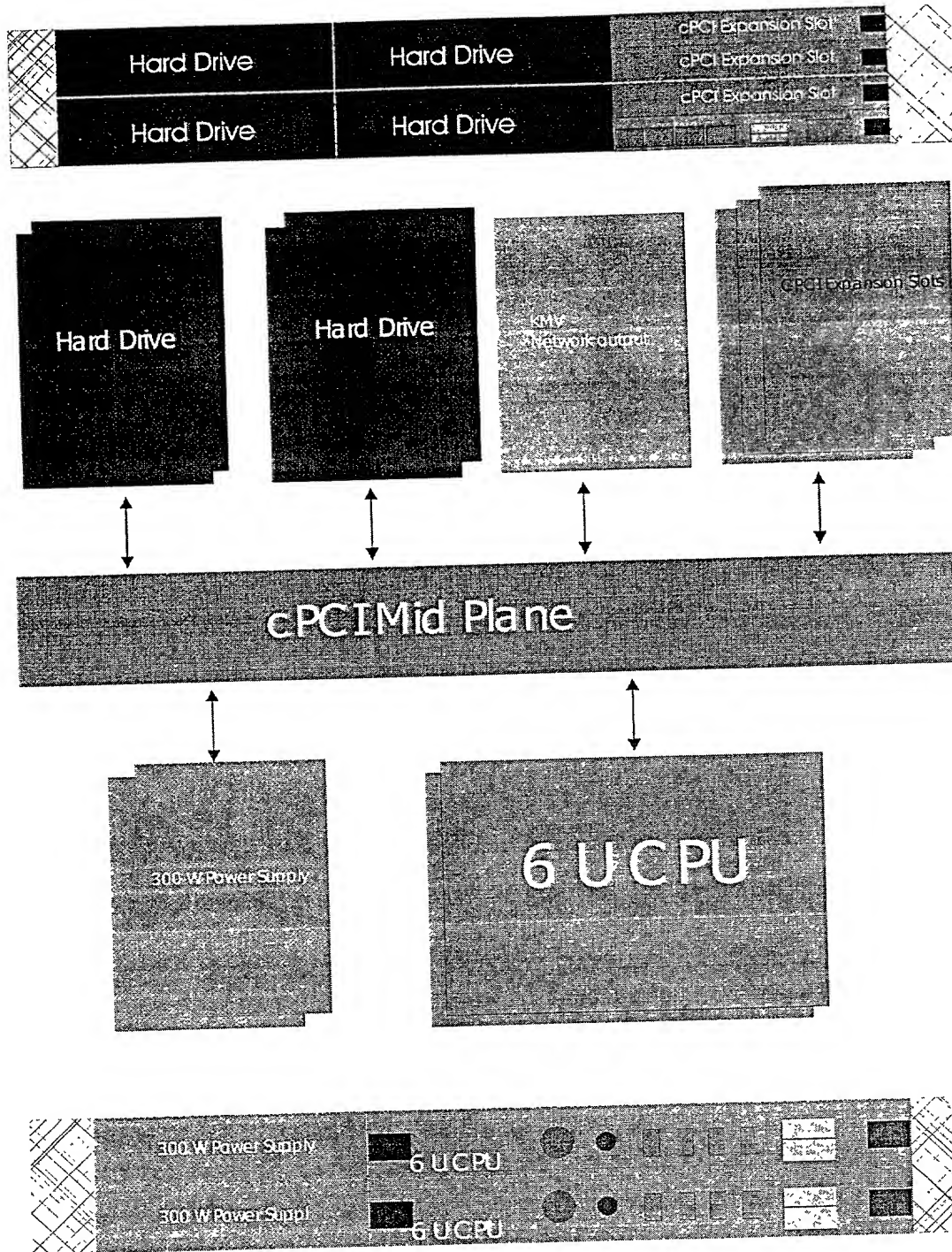


FIG. 13

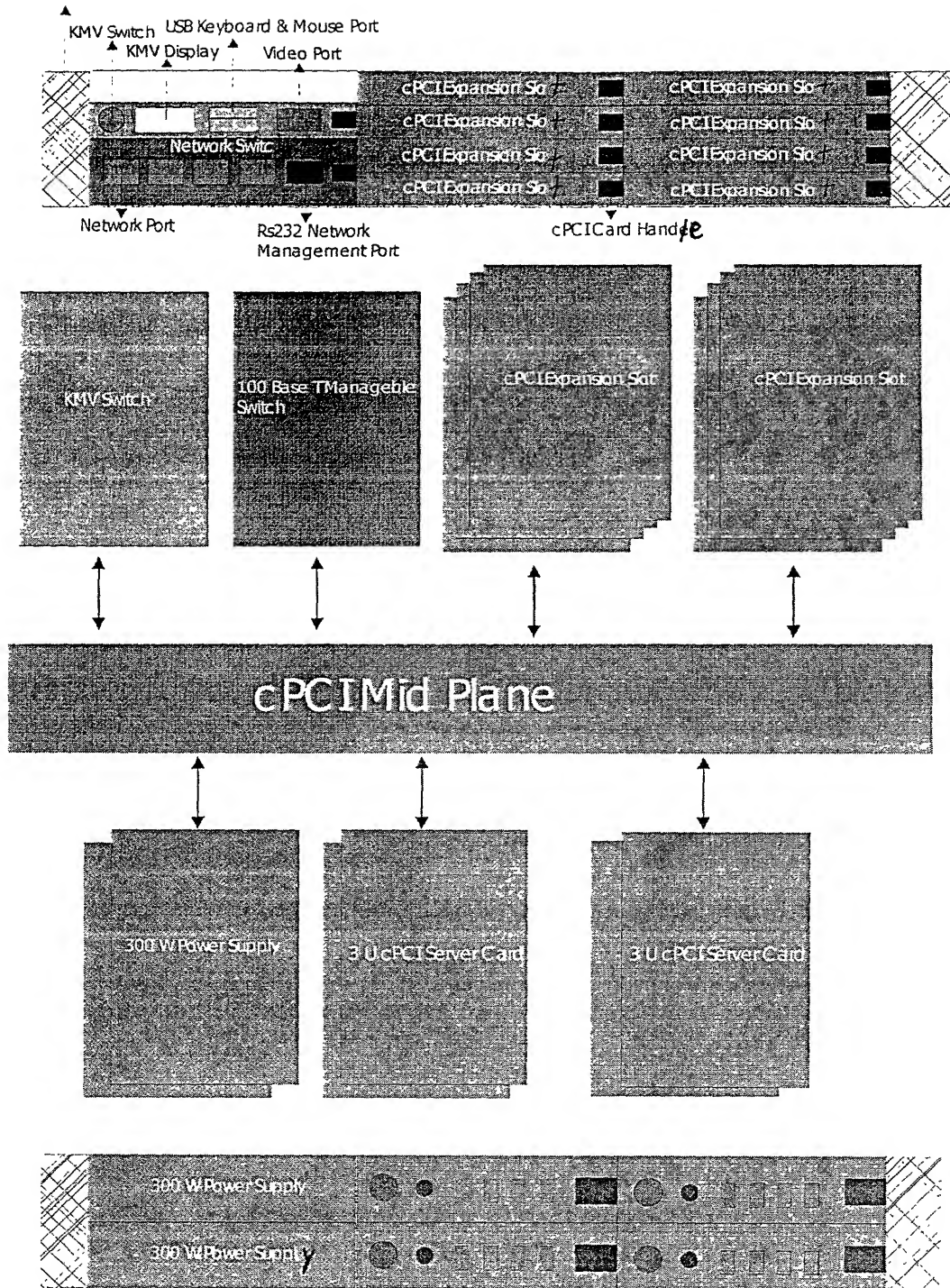


FIG. 14

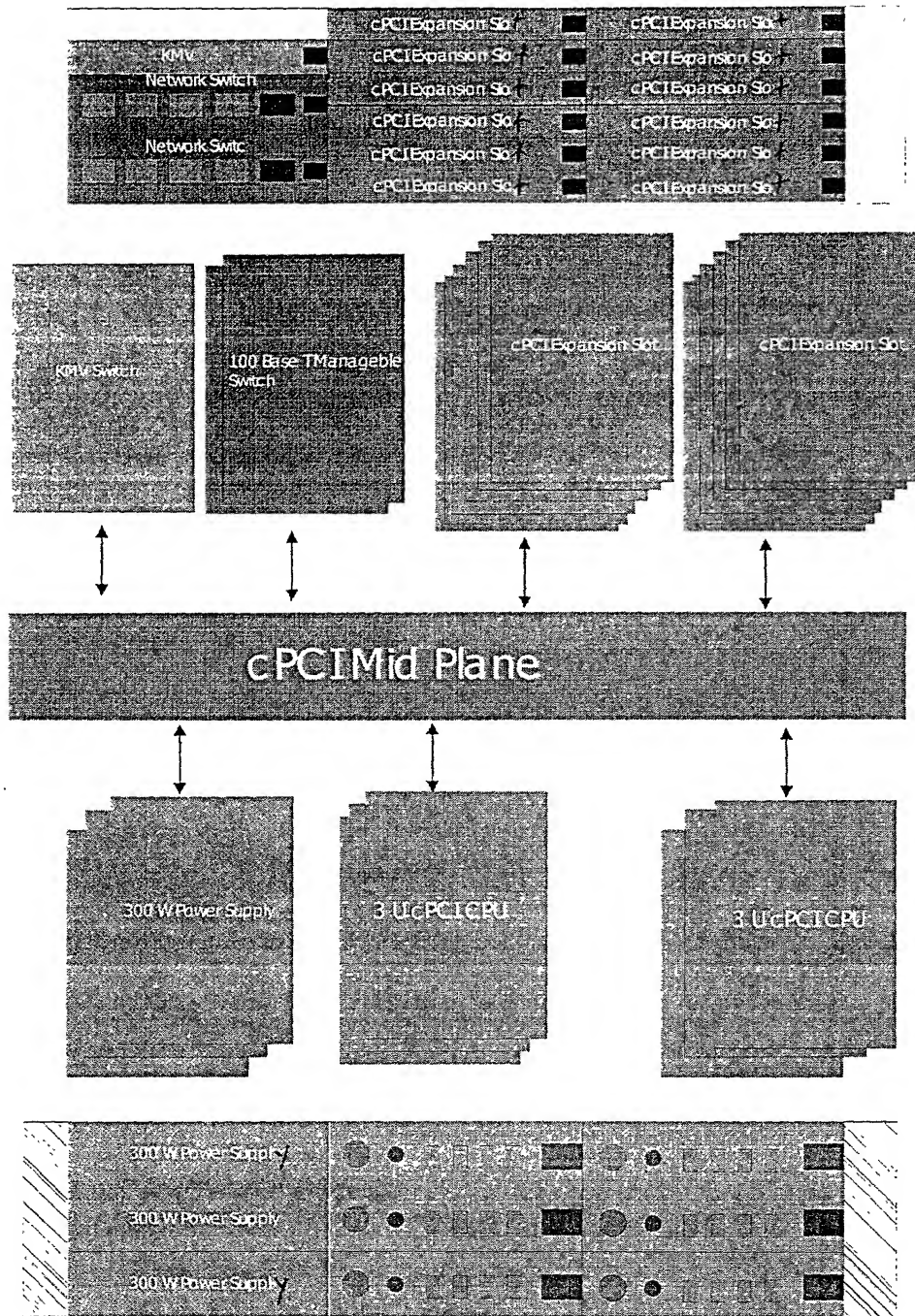


FIG. 15

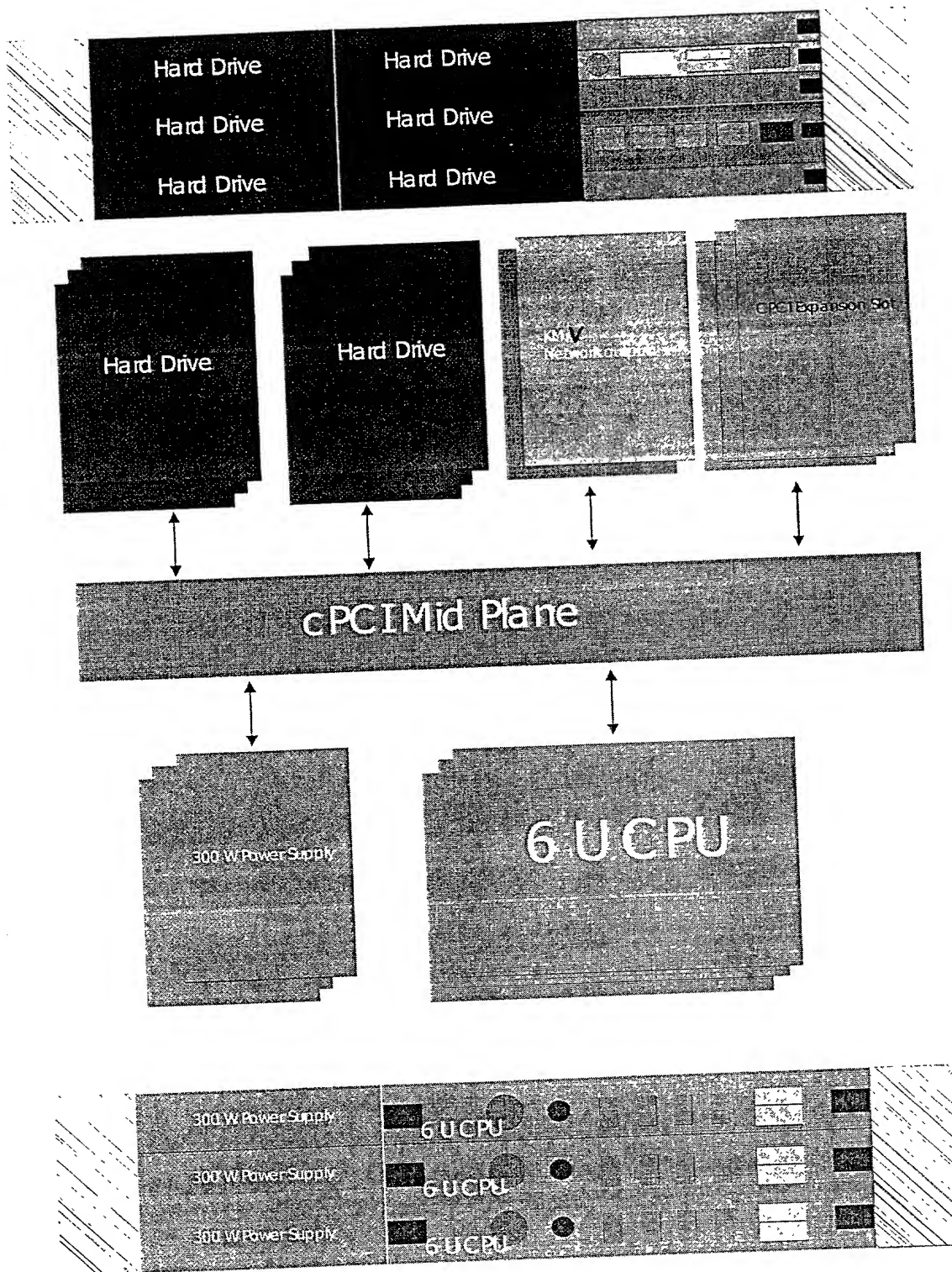


FIG. 16

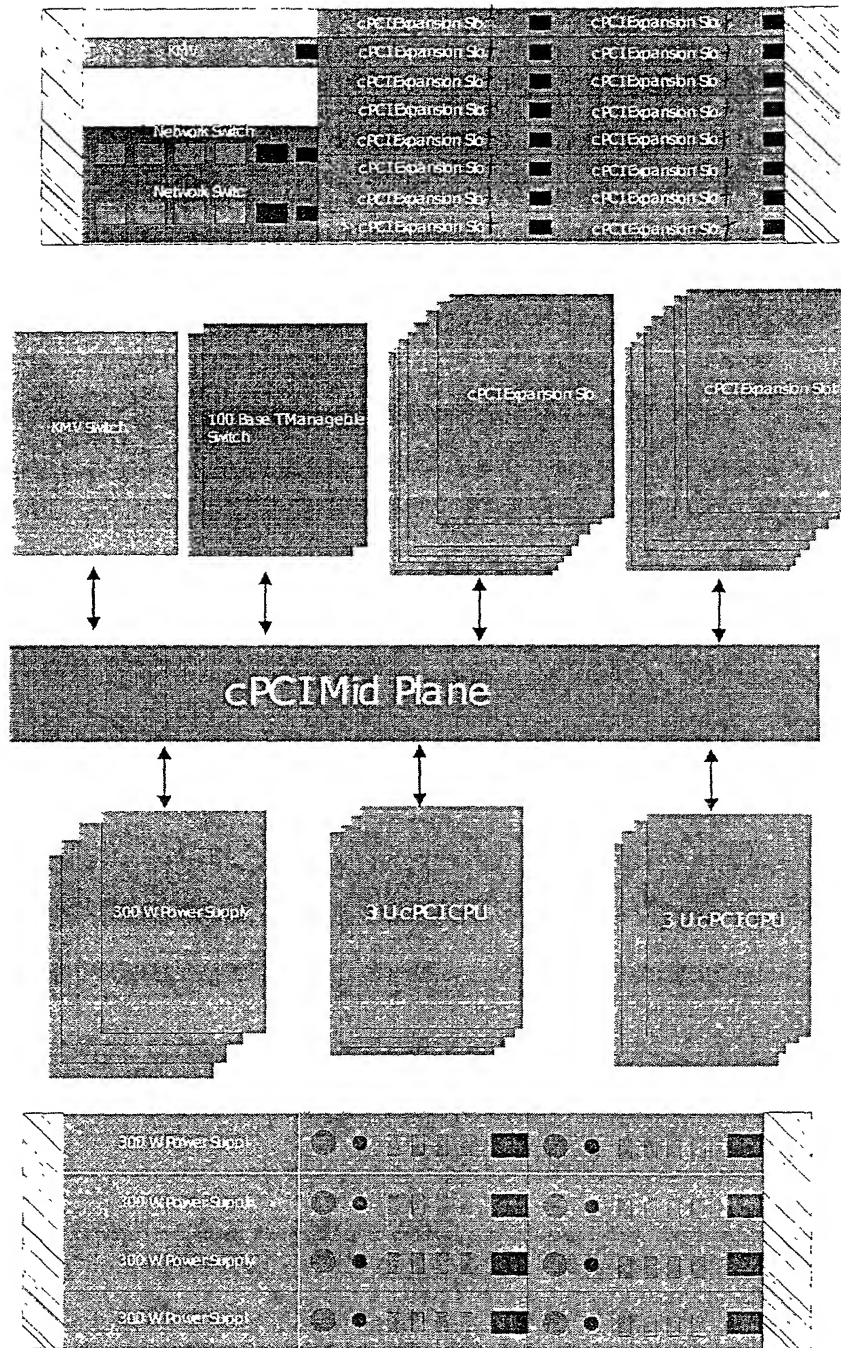


FIG. 17

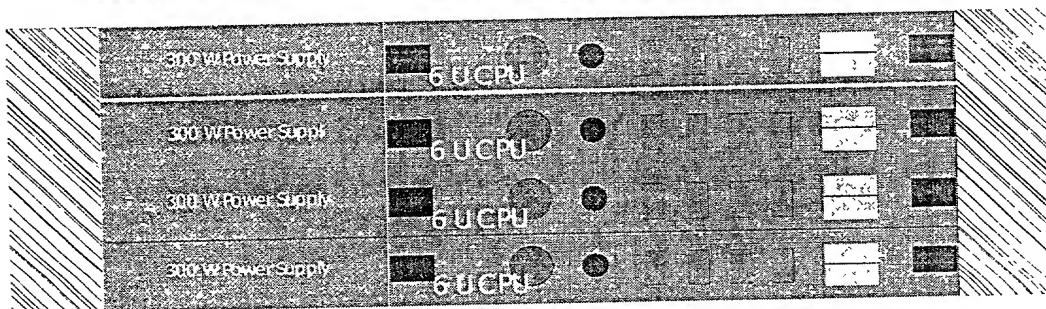
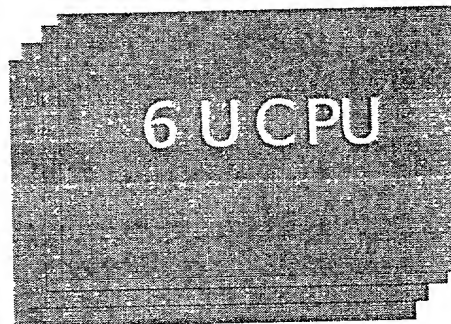
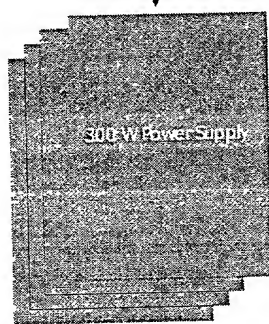
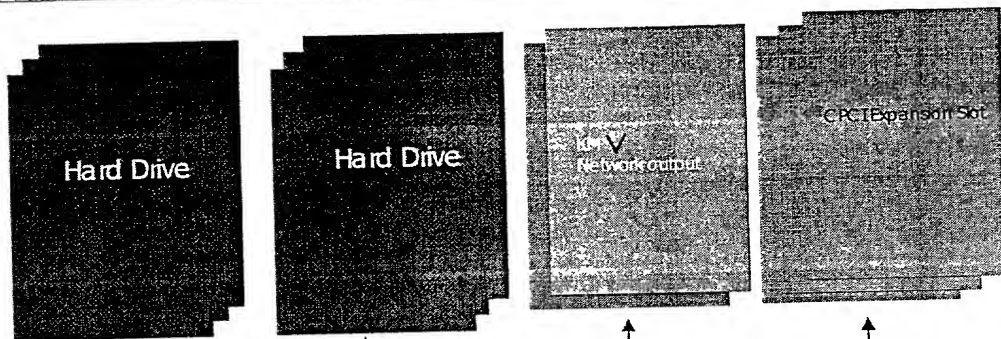
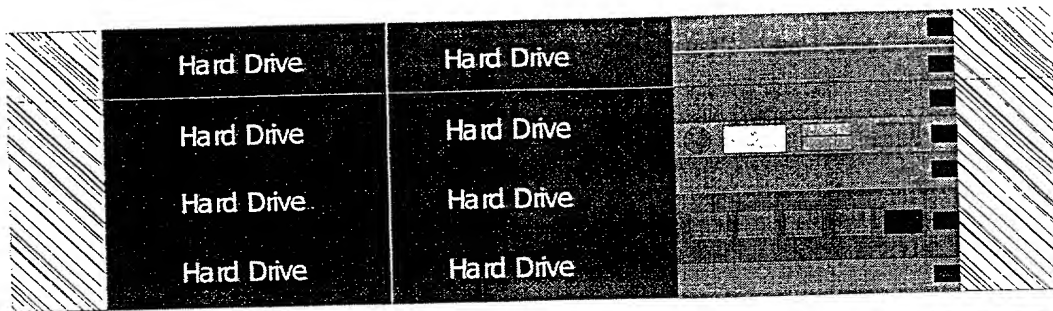


FIG. 18

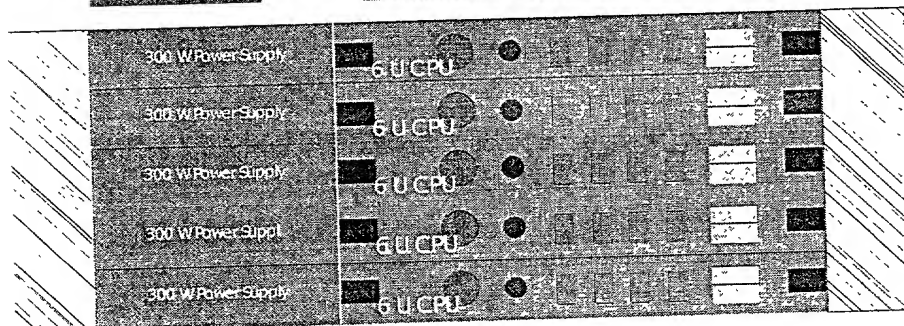
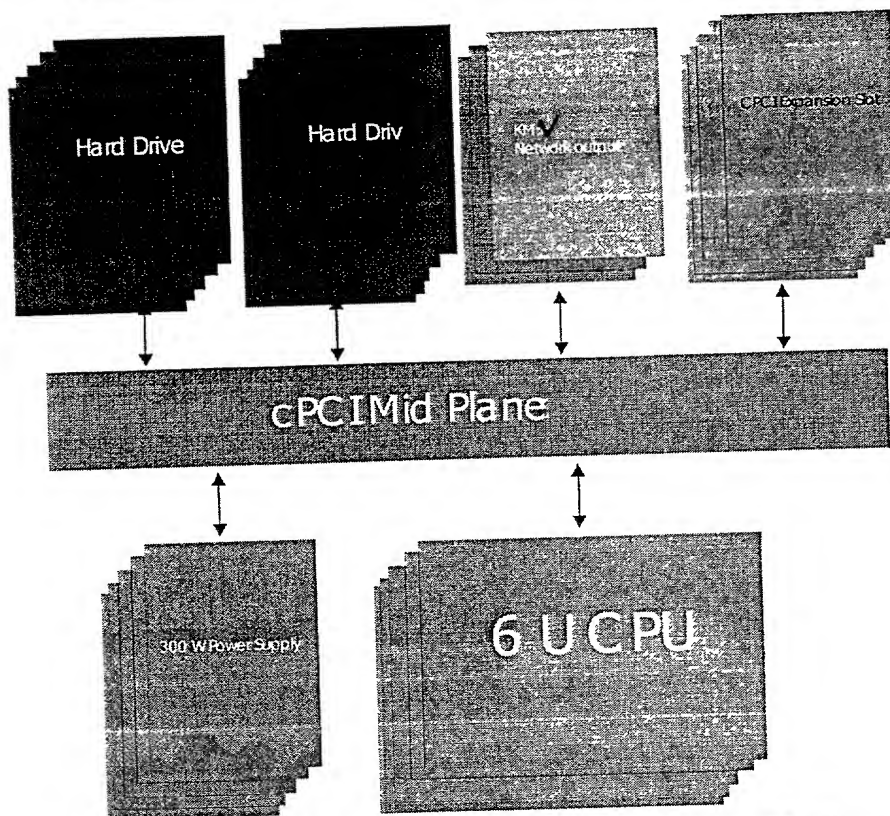
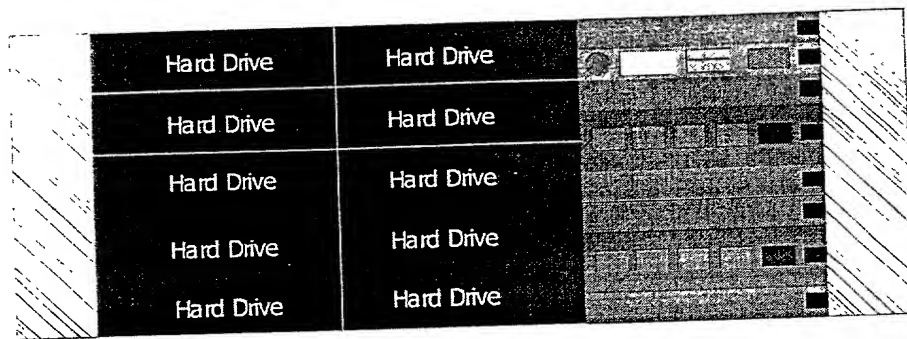


FIG. 19

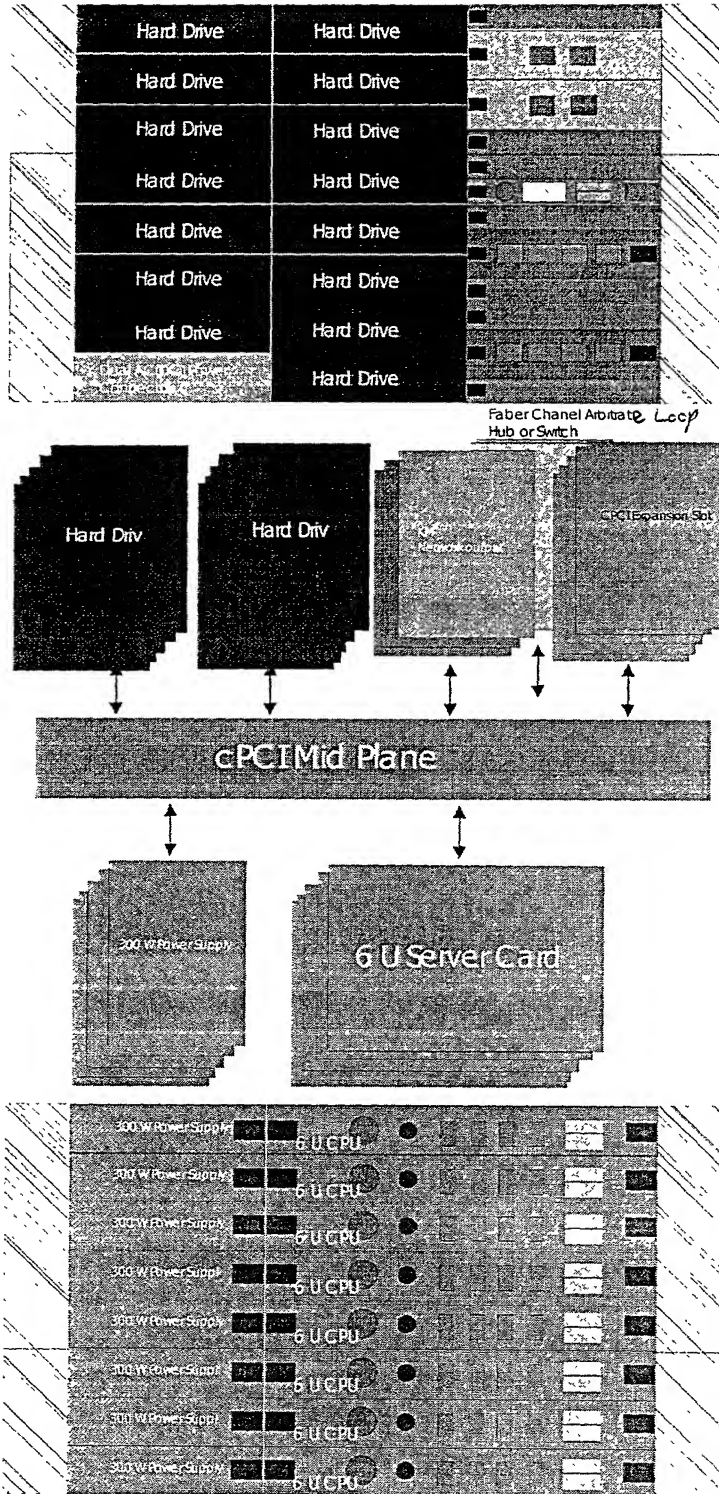


FIG. 20

Fig. 21

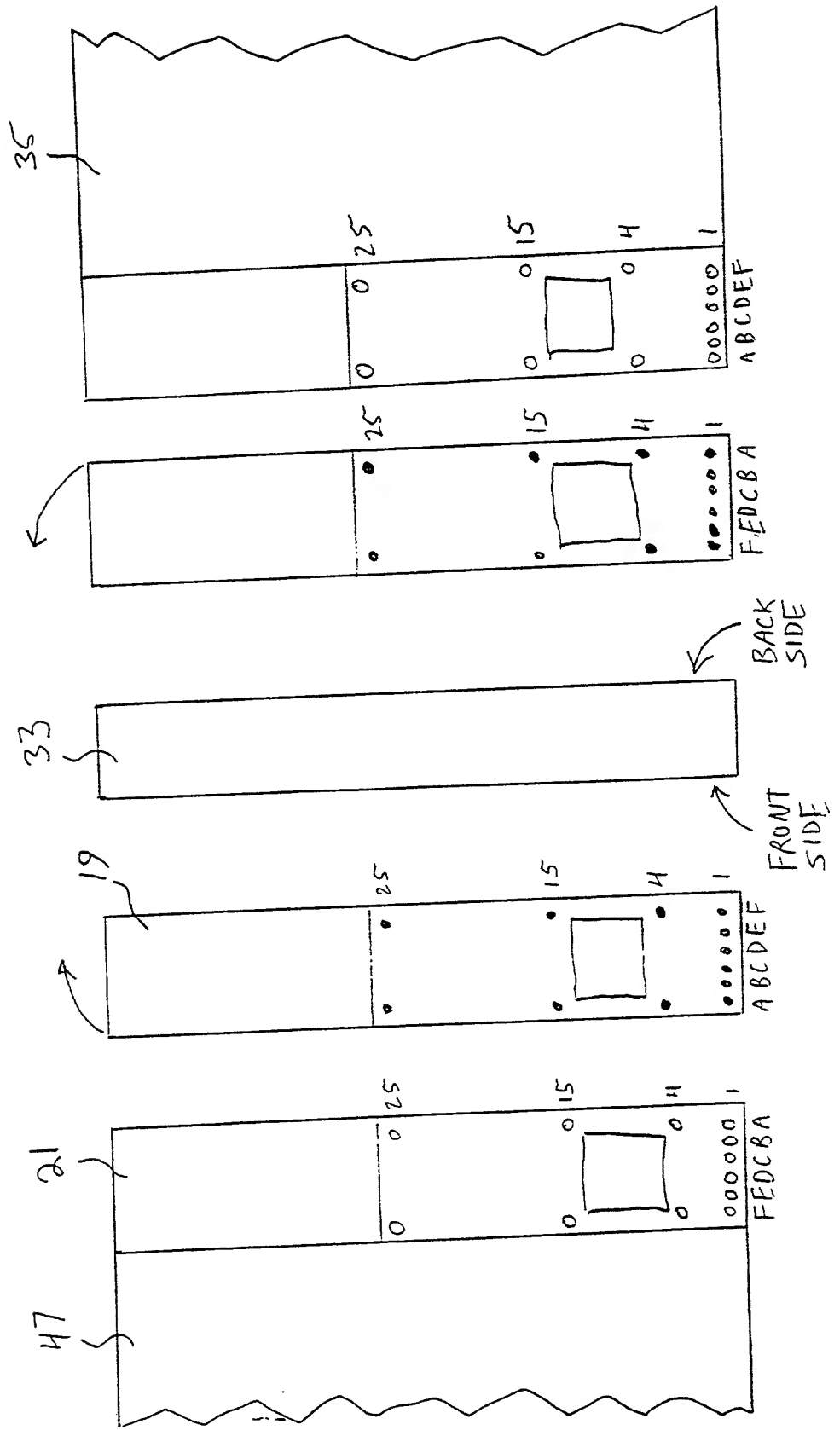


Figure 22 shows a plan view of the layout of the components on the printed circuit board. The components are arranged in a grid pattern, with the components in the center of the board being larger than the components on the edges. The components are labeled with their respective designations, such as C1, C2, C3, C4, C5, C6, C7, C8, R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, R17, R18, R19, R20, and J1. The components are arranged in a grid pattern, with the components in the center of the board being larger than the components on the edges.

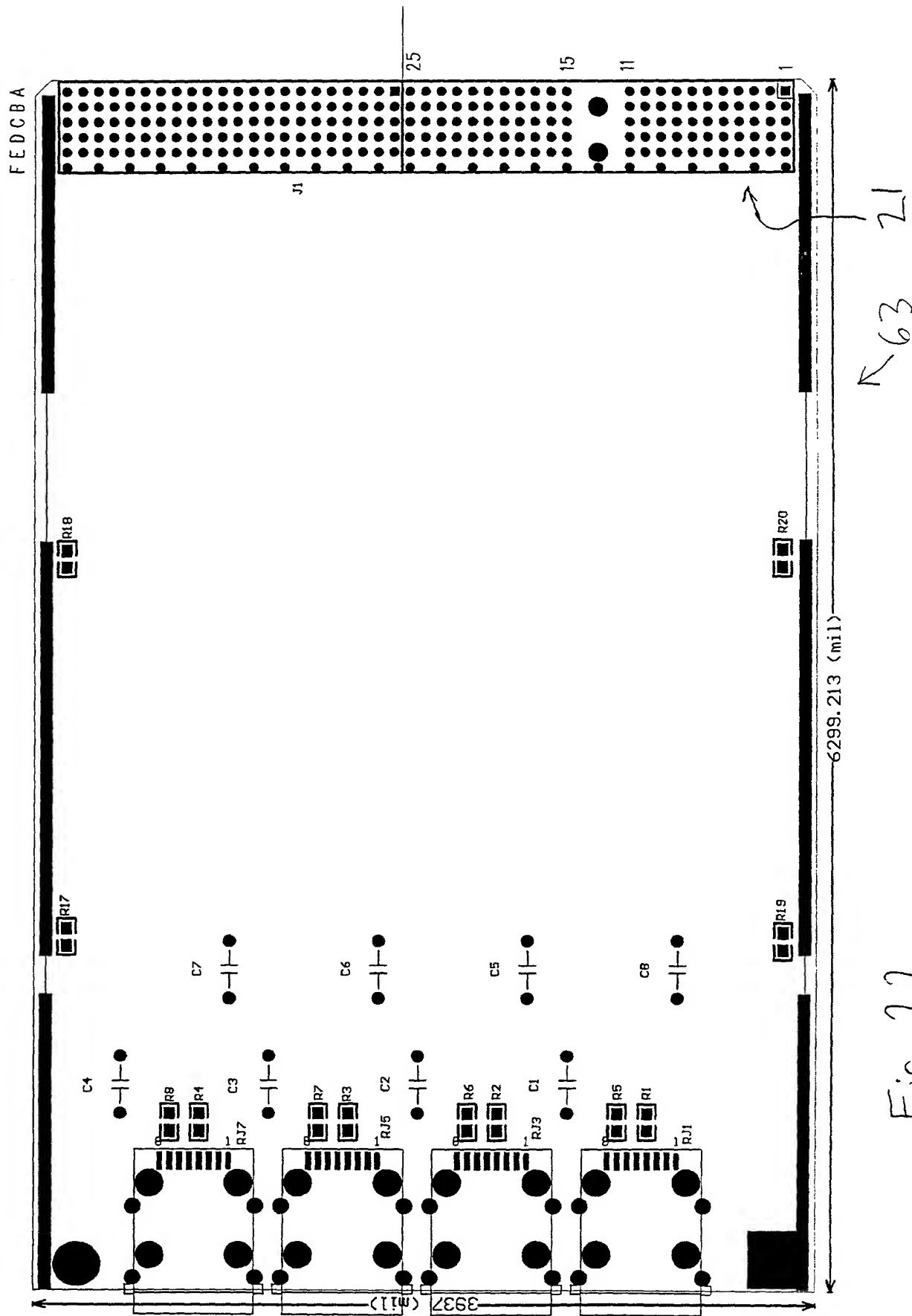


Fig. 22

FIG. 23 is a schematic diagram of a system for monitoring a process. The system includes a process 10, a sensor 12, a controller 14, and a display 16. The sensor 12 is connected to the controller 14, which is connected to the display 16. The controller 14 is also connected to the process 10. The display 16 displays information about the process 10.

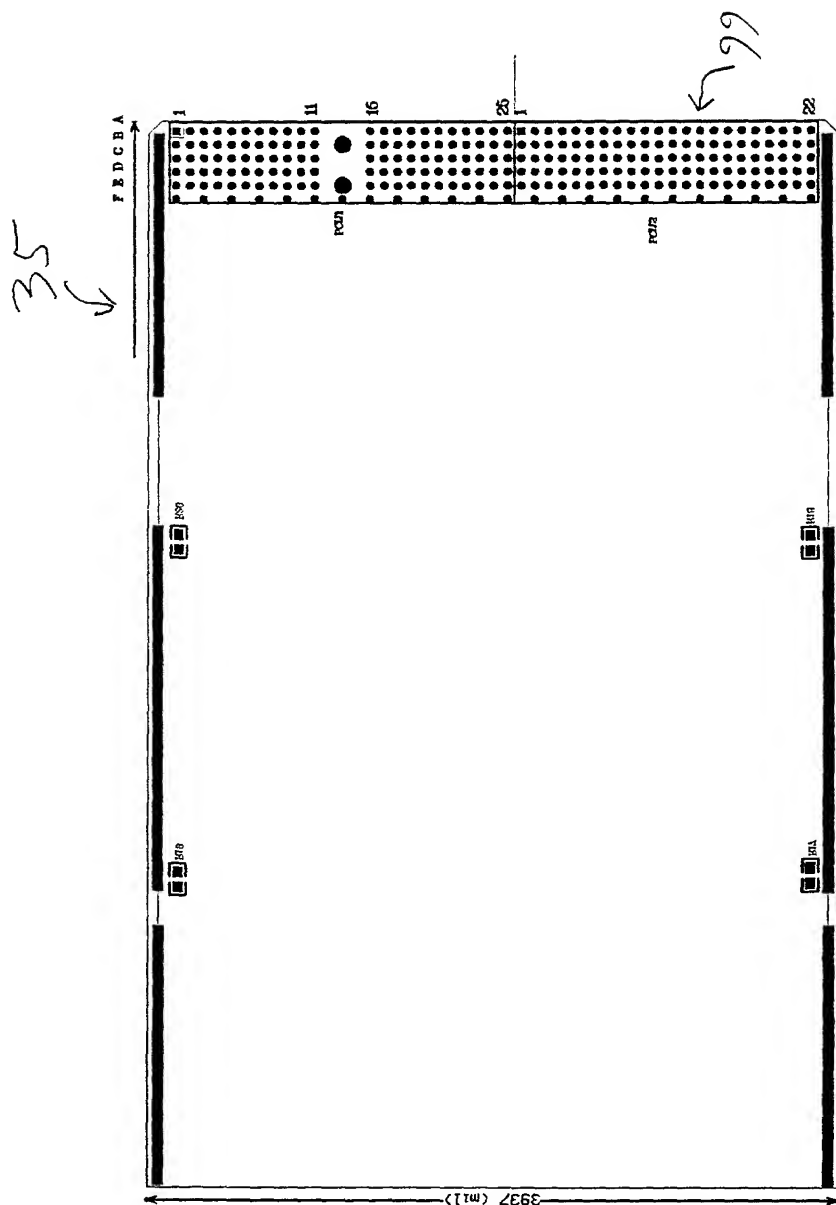


Fig. 23

22	GND	GND	GND	GND	GND	GND	GND	J2
21	GND	?3	GND	?18	?24	SMBDAT	GND	
20	GND	?2	?7	?17	GND	SMCLK	GND	
19	GND	GND	GND	?15	?22	CUV1+	GND	
18	GND	MDCLK	?5	?14	GND	GND	GND	C
17	GND	GND	GND	?13	?21	CUV1-	GND	
16	GND	MDDAT	MVSYNC	?12	GND	GND	GND	
15	GND	GND	GND	?11	?20	?28	GND	
14	GND	RSTSW#	MHSYNC	VCC5IN	GND	?27	GND	O
13	GND	GND	GND	VIO	ER1+	GND	GND	
12	GND	CUV0-	MB	VCC5IN	GND	ER2+	GND	
11	GND	GND	GND	VIO	ER1-	GND	GND	
10	GND	CUV0+	MG	VCC5IN	GND	ER2-	GND	E
9	GND	GND	GND	VIO	ET1+	GND	GND	
8	GND	MUSDATA	MR	VCC5IN	GND	ET2+	GND	
7	GND	GND	GND	VIO	ET1-	GND	GND	
6	GND	MUSCLK	?10	VCC5IN	GND	ET2-	GND	T
5	GND	GND	?9	VIO	?26	GND	GND	
4	GND	VIO	?8	VCC5IN	GND	CUV3-	GND	
3	GND	?4	GND	?19	?25	GND	GND	
2	GND	?1	?6	?16	?23	CUV3+	GND	R
1	GND	PCICLK4	GND	PREQ# 3	PGNT# 3	GND	GND	
Pin	Z	A	B	C	D	E	F	

FIG. 24